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The World's Smallest Cell Implementation for a High-Density Standby-Power-Free TCAM in Combination with Silicon/Magnetic Devices

[Abstract] A research group of Professor Hideo Ohno, Professor Takahiro Hanyu of Center for Spintronics Integrated Systems, and Research Institute of Electrical Communication of Tohoku University and NEC Corporation (NEC) developed the world's smallest fully parallel ternary content-addressable memory (TCAM) cell. By using a spintronics-based nonvolatile logic-in-memory circuit technique, which can compactly merge storage and logic functions into a silicon-device/spintronics-device-combined integrated circuit, the developed nonvolatile TCAM cell circuit has been miniaturized with the smallest device counts. A test chip was successfully fabricated using a 300-mm wafer fabrication line ^{*1)} for a spin-transfer-torque (STT)-type magnetic tunnel junction (MTJ) device ^{*2)} and a 90-nm standard silicon CMOS fabrication line in collaboration with NEC. The TCAM chip is utilized for high-speed searching hardware such as network routers, virus checkers, and databases. The success of this technology will accelerate the development of not only ultra-low-power System-on-a-Chips, which are utilized in almost all the electronic equipments as artificial intelligent controllers like a brain, but also a larger-scaled integration.

[Background]

Reducing power consumption and reducing interconnection delay are the two major targets for the next generation VLSIs. Drastic increase in static power dissipation is anticipated due to leakage current in beyond 45-nm CMOS technology. In addition, lengthening the global-interconnection in advanced VLSIs further increases both power and delay.

A ternary content-addressable memory (TCAM) is an attractive hardware engine with its high-speed fully parallel data search. It is useful in a number of applications such as IP filters, network switches, look-up tables, and virus checkers. However, the TCAM consisting of a volatile CMOS-based 16-transistor (16T) or 12T cell circuit has two major issues. One is its increasing standby power due to leakage current in nanometer-scaled CMOS era. The other is its high bit-cell cost, because the TCAM cell needs 2-bit storage elements and a comparison logic element. Therefore, it is important to achieve a low standby power and compact TCAM while maintaining high-speed operation.

Professor Hideo Ohno (Tohoku University), who has the highest level technologies to make spintronics devices, and Professor Takahiro Hanyu (Tohoku University), who has anticipated the nonvolatile logic-in-memory circuit techniques, ^{*3)} have collaborated through the MEXT programs ^{*4)} since 2005. One of the successful results of this research collaboration has been to develop successfully a compact nonvolatile TCAM chip that can perform a fully parallel search operation with a low magnetic-resistance ratio at the present MTJ devices. This result was presented in the VLSI Circuit Symposium 2011. "Immediate wake up" behavior and "complete standby power-off" have been combined in the fabricated prototype chip, which may accelerate the development of nonvolatile System-on-a-Chips.

[Research issue]

In general, it is difficult to achieve a high-density TCAM because its cell circuit needs a 2-bit storage function and a comparison logic function, which causes larger cell area than SRAM as a representative embedded memory. A modern information-intensive society has a drastically increased amount of information with which to deal. Hence, achieving a higher and higher density of TCAM is one important challenge. Moreover, power consumption in VLSI chips, especially standby power consumption, has increased remarkably due to the leakage current in accordance with CMOS technology scaling. Thus, it is also an important challenge to reduce standby power consumption in TCAM. From these points of view, it is essential not only to suppress the TCAM cell area extremely but also to cut down its standby power consumption.

[Technical method and achievement]

They developed a smaller nonvolatile TCAM cell by using silicon-device/MTJ-device-hybrid nonvolatile logic-in-memory architecture that they had previously proposed.

The new TCAM cell circuit is achieved with reduced transistor counts by maximally sharing cell transistors and cell wires from the previous cell circuit (6T-2MTJ: 6-transistor and 2-MTJ-device structure), which has been reported at the IEEE VLSI Circuit Symposium, June 2011. As the result, a compact nonvolatile TCAM cell circuit is achieved with a 4T-2MTJ structure, which has smaller transistor counts than a SRAM cell circuit.

This achievement opens up the potential capability for a high-density nonvolatile TCAM.

[Significance of research]

To overcome the problems in miniaturizing the cell size and lowering its power consumption, silicon-device/MTJ-device-hybrid nonvolatile logic-in-memory circuit technique together with spintronics material/process/device techniques are utilized.

In the silicon-device/MTJ-device-hybrid integrated circuits, the transistors and wires for writing data to MTJ devices are alternatives to those for reading data from the MTJ devices. From this point, those transistors and wires can be shared for both write and read phases. In the developed cell circuit, all the transistors are perfectly shared for both data write and read (equality-search) operations. Cell wires are also perfectly shared in both phases. By optimizing the cell structure, transistor counts of the cell circuit are minimized to a 4T-2MTJ structure. This cell circuit consists of smaller transistor counts than a SRAM cell as a representative embedded memory while requiring nonvolatility for perfectly cutting down standby power consumption.

These results indicate that fundamental techniques for an ultimate high-density nonvolatile TCAM have been achieved.

Tohoku University and NEC will announce their latest results on June 13 at the VLSI Circuit Symposium 2012 (June 12-15, Hawaii, USA).

This research was funded by the Japan Society for the Promotion of Science (JSPS) through the “Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program),” initiated by the Council for Science and Technology Policy (CSTP).

Notes:

*1) Super Clean-Room (SCR) in Tsukuba Innovation Arena (TIA)

*2) STT-type MTJ device

STT-type MTJ devices are superior spintronics devices that have been progressively developed in Prof. Hideo Ohno's research group.

*3) Nonvolatile logic-in-memory circuit technique

In this architecture, developed by W. H. Kautz in 1969, storage elements are distributed over a logic-circuit plane. Combining this architecture and nonvolatile storage elements makes it possible to reduce the hardware overhead due to logic-in-memory architecture by replacing storage elements to nonvolatile ones and to implement the circuit compactly by merging storage and logic functions.

*4) From 2002 to 2006: Information Technology program of the Research Revolution 2002 (RR2002) from the Ministry of Education, Culture, Sports, Science and Technology (MEXT) of Japan. Prof. Takahiro Hanyu joined this program in 2005.
From 2007 to 2009: Research and Development for Next-Generation Information Technology by the Ministry of Education, Culture, Sports, Science and Technology (MEXT) of Japan.

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